Ex parte Reiffen

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

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Paper No. 46

JUN 13 1995

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BOARD OF PATENT APPEALS
AND INTERFERENCES

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MARTIN G. REIFFIN

Appeal No. 94-1471
Application 07/496,282[1]

ON BRIEF

Before HARKCOM, Vice-Chief Administrative Patent Judge, and HAIRSTON and FLEMING, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

REQUEST FOR RECONSIDERATION

Appellant has requested reconsideration of our decision dated October 5, 1994, wherein we entered new grounds of

[1] Application for patent filed March 20, 1990. According to applicant, the application is a continuation-in-part of Application 06/425,612, filed September 28, 1982.

rejection of claim 59 under 37 CFR 1.196(b). As indicated on pages 6 through 8 of the decision, the claimed subject matter directed to "asynchronously" interrupting execution of the threads was found to be misdescriptive and, thus, indefinite under the second paragraph of 35 U.S.C. § 112. In addition, the now claimed subject matter was found to lack support in the originally filed disclosure under the first paragraph of 35 U.S.C. § 112.

In the second full paragraph on page 3 of the request, appellant argues that the disclosed compiler thread and editor thread run concurrently without any timing relationships. Inasmuch as the claimed interruption of the first thread is under the control of the claimed "clock means," we do not find any merit in appellant's argument, and in his reliance on Exhibit B and Exhibit G. The claimed "clock means" is at odds with the Exhibit G statement that asynchronously executed threads are "run simultaneously but without timing relationships." (Emphasis added). The Exhibit B description on page 2 of the request likewise fails to take into consideration the claimed "clock means." More importantly, the Exhibit B and Exhibit G descriptions of the term "asynchronous" in the multithreading art are diametrically opposed to the arguments made by appellant in the briefs to overcome the prior art rejections of claims 59, 62 and 64.

We have carefully considered appellant's arguments in the request, and we do not find any error in the new rejections under 37 CFR 1.196(b). Accordingly, appellant's request has been granted to the extent that our decision has been reconsidered, but such request is denied with respect to making any modifications to the decision.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR 1.136(a).

RECONSIDERATION
DENIED

GARY V. HARKCOM, Vice-Chief
Administrative Patent Judge

KENNETH W. HAIRSTON
Administrative Patent Judge

MICHAEL R. FLEMING
Administrative Patent Judge

BOARD OF PATENT
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Paper No. 44

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MARTIN G. REIFFIN

Appeal No. 94-1471
Application 07/496,282[1]

ON BRIEF

Before HAIRSTON, HARKCOM and FLEMING, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1 through 13, 16 through 22, 29, 30, 32, 33, 37, 38, 41 through 51 and 55 through 64. A first Amendment After Final (paper number 9) was denied entry, and in a second Amendment After Final (paper number 14), claims 10 through 13, 37, 38, 42, 48 through 51, 56

[1] Application for patent filed March 20, 1990. According to applicant, the application is a continuation-in-part of Application 06/425,612, filed September 28, 1982.

and 58 were cancelled, and claims 1, 9, 16, 29, 30, 41, 43, 44, 46, 47, 55, 57, 59, 61 and 62 were amended. In a third Amendment After Final (paper number 16), claims 41 and 43 were amended. A fourth Amendment After Final (paper number 27) was denied entry, and in a fifth Amendment After Final (paper number 32), claims 60, 61 and 63 were cancelled, and claims 81 through 83 were substituted for these cancelled claims. In an Advisory Action (paper number 34), the examiner indicated that claims 81 through 83 were allowable along with claims 1 through 9, 16 through 22, 26, 27, 29, 30, 32, 33, 39, 41, 43 through 47, 52 through 55 and 57. Accordingly, claims 59, 62 and 64 remain before us on appeal.

The disclosed invention relates to a multithreading software-programmable general purpose computer system for concurrent processing and modification of a body of data code by at least two concurrently executing instruction threads constituting a single program.

Claim 59 is illustrative of the claimed invention, and it reads as follows:

59. A multithreading software-programmable general-purpose computer system for concurrent processing of the same body of data code by at least two concurrently executing instruction threads constituting a single program, said computer system comprising:

a central processing unit having an interrupt input,

a memory,

means for entry into said memory of a body of data code to be processed,

means for operator selection and entry into said memory of a program comprising at least two concurrently executable instruction threads for processing said body of data code,

means to cause the central processing unit to execute a first of said entered threads under control of said first thread to process the previously entered body of data code in accordance with a first mode of processing,

clock means to repeatedly activate said interrupt input so as to asynchronously interrupt execution of said first thread and preemptively switch control of the central processing unit to another of said entered threads for execution of said another thread so as to process the same previously entered body of data code in accordance with a second mode of processing, and

means activated after each said interrupt input activation and its respective second mode of processing by said another thread to return control of the central processing unit to said first thread to enable said first thread to resume said first mode of processing said body of data code at the point in the code where the first thread had been interrupted.

The reference relied on by the examiner is:

Maddock 4,513,391 Apr. 23, 1985

Claim 62 stands rejected under 35 U.S.C. 102(e) as being anticipated by Maddock.

Claims 59 and 64 stand rejected under 35 U.S.C. 103 as being unpatentable over Maddock.

Reference is made to the briefs and the answers for the respective positions of the appellant and the examiner.

OPINION

We have carefully considered the entire record before us, and we will reverse the prior art rejections of claims 59, 62

and 64. New grounds of rejection of claim 59 are entered under 37 CFR 1.196(b).

Appellant argues in the briefs that the claims on appeal recite a multithreading general-purpose computer system that concurrently executes at least two instruction threads. According to appellant, the claimed computer system has means for repeatedly activating an interrupt input to a central processing unit to preemptively switch control of the central processing unit from one thread to the other thread during execution of the concurrently executing instruction threads. Claims 59 and 64 include clock means for repeatedly activating the interrupt input to the central processing unit. The clock means in claim 59 repeatedly activates the interrupt means so as to asynchronously interrupt execution of one thread in favor of the other thread. Of course, appellant argues that the reference to Maddock neither teaches nor would it have suggested any of these claimed features.

Attachment B to the answer defines multithread processing as parallel processing of threads. The reference to Maddock discloses apparatus that performs text editing and reformatting in two separate stages run as two parallel processes. Inasmuch as the text editing and reformatting in

Maddock are run as two parallel processes, we agree with the examiner that multithreading is disclosed in Maddock. A keystroke is used by Maddock to preemptively switch from one process to another process. On page 13 of the main brief, appellant acknowledges that the interrupt handler 14 in Maddock operates in an asynchronous manner. Notwithstanding the examiner's demonstration that multithreading is disclosed in the reference to Maddock, the form of multithreading in Maddock is not the same multithreading set forth in the claims on appeal. For example, the two threads in Maddock are executed in sequence or one after the other, and never in a concurrent manner as required by claims 59, 62 and 64. The Abstract of the disclosure in Maddock clearly states that the reformatting is subsequent to the text editing. The subsequent processing of the reformatting or background process is discussed by Maddock at column 5, lines 44 through 46, and at column 7, lines 31 through 33 wherein it is stated that the background reformatting is run upon completion of the foreground process. Another difference between the multithreading disclosed by Maddock and the claimed multithreading is the clock means in claims 59 and 64. The examiner's contentions at page 8 of the supplemental answer (paper number 35) to the contrary notwithstanding, the keyboard interrupt in Maddock is not a clock. Since keyboard strikes are usually random, as opposed to timed, we are not convinced by the

examiner's reasoning that an interrupt caused by the striking of a key on a keyboard is "a clock measuring the passage of time in that it is measuring the passage of time between each keystroke made upon the keyboard." For this reason, we agree with the appellant that the use of such a keyboard interrupt would not have suggested a clock means as set forth in the claims on appeal.

The 35 U.S.C. 102(e) rejection of claim 62 is reversed because the reference to Maddock does not teach concurrently executing threads, and the 35 U.S.C. 103 rejection of claims 59 and 64 is reversed because the reference to Maddock neither teaches nor would it have suggested to the skilled artisan concurrently executing threads and clock means.

Pursuant to the provisions of 37 CFR 1.196(b), we hereby enter the following new rejections:

In claim 59, the clock means is required to asynchronously interrupt execution of one thread in favor of another thread. When the claim is considered as a whole in a vacuum, it appears to set out and circumscribe a particular area with a reasonable degree of precision. On the other hand, when the claim is read in light of the disclosure and relevant prior art, it becomes abundantly clear to us that the originally filed disclosure is completely silent concerning an "asynchronously" interrupted execution of the threads. Nothing in the paragraph

bridging pages 20 and 21 of the specification would teach or suggest such asynchronously interrupted execution of the threads by the clock/timer. On page 11 of the main brief, appellant argues that an "inherent characteristic of multithreading is that it is asynchronous." Appellant's evidence of such asynchronous execution of the threads is the Young publication (Exhibit G attached to appellant's fourth affidavit) which bears a publication date of 1988. As indicated by the examiner in the answer, a publication with a date subsequent to appellant's original filing date can not be relied on to establish a so-called inherent characteristic of the disclosed and claimed multithreading process. The multithreading definition cited by the examiner certainly does not mention asynchronous execution of the threads. Accordingly, the claimed subject matter directed to "asynchronously" interrupting execution of the threads is inconsistent with what has been disclosed, and it is misdescriptive and, thus, indefinite. See In re Cohn, 438 F.2d 989, 169 USPQ 95 (CCPA 1971). In addition, the originally filed disclosure would not have reasonably conveyed to one having ordinary skill in the art that appellant had possession of the now claimed subject matter directed to "asynchronously" interrupting execution of the threads. Accordingly, claim 59 is rejected under the second paragraph of 35 U.S.C. 112 as being indefinite, and under the first paragraph of 35 U.S.C. 112 as

lacking written description support in the originally filed disclosure.

DECISION

The decision of the examiner rejecting claim 62 under 35 U.S.C. 102(e), and claims 59 and 64 under 35 U.S.C. 103 is reversed. New grounds of rejection of claim 59 have been entered under 37 CFR 1.196(b).

Any request for reconsideration or modification of this decision by the Board of Patent Appeals and Interferences based upon the same record must be filed within one month from the date of the decision (37 CFR 1.197). Should appellant elect to have further prosecution before the examiner in response to the new rejections under 37 CFR 1.196(b) by way of amendment or showing of facts, or both, not previously of record, a shortened statutory period for making such response is hereby set to expire two months from the date of this decision.

Effective August 20, 1989, 37 CFR 1.196(b) has been amended to provide that a new ground of rejection pursuant to the rule is not considered final for the purpose of judicial review under 35 U.S.C. 141 or 145.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR 1.136(a).

REVERSED
37 CFR 1.196(b)

KENNETH W. HAIRSTON
Administrative Patent Judge

GARY V. HARKCOM
Administrative Patent Judge

MICHAEL R. FLEMING
Administrative Patent Judge

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